DESCRIPTION AMENDMENTS

Insert the following new paragraph following the paragraph beginning on page 3, line 8:

Fig. 4 is a simplified functional block diagram illustrating the demultiplexer and a system target decoder.

Rewrite the paragraph beginning on page 4, line 4, to read as follows:

~~The SPTS(VBR) is separated~~ Referring to Fig. 4, the MPTS is delivered to a demultiplexer 2 for separation into multiple single program transport streams (SPTSs). The demultiplexer separates Program 1 from the ~~MTS~~ MPTS based upon the packet PIDs, and ~~is input to~~ loads Program 1 into a logical smoothing buffer ~~for output for decoding~~ 4 at the desired constant bitrate. The buffer 4 outputs Program 1 to produce an SPTS having a Constant Bit Rate (CBR). The SPTS (CBR) may then be decoded at the time indicated by the decode time stamp (DTS) for each frame to recover the original images in the video stream.

Rewrite the paragraph beginning on page 6, line 11, to read as follows:

The above is illustrated in Fig. 3 where a series of frames of variable bit rates is shown. In this explanation, DTS_j is the decode time stamp for frame j, i.e. $td_n(j)$, and Q_j is the size in bits of frame j. At time δ before ~~the DTS for frame 1, frame 1 is loaded~~ DTS_1, frame 1 begins loading into the buffer and continues loading until time $\delta + R_n*Q_1$ before DTS_1. The buffer may be thought of as having a plurality of equal capacity slots between consecutive DTS times. Since frame 1 has fewer bits than the capacity of one slot, R_n*Q_1 is less than DTS_2-DTS_1 and there is a gap before frame 2 ~~is loaded~~ starts loading into the buffer, ~~again~~ at time δ before ~~the DTS for frame 2~~ DTS_2. Likewise frame 3 ~~is loaded~~ starts loading at time δ before DTS_3. Frame 3 has more bits than fit into one slot, so ~~that~~ R_n*Q_3 is greater than DTS_4-DTS_3 and frame 3 does not finish loading until after time δ before DTS_4. Consequently, frame 4 ~~is loaded~~ begins loading into the buffer as soon as possible ~~thereafter~~ after loading of frame 4 is complete. Then frame 5 ~~is loaded~~ begins loading into the buffer as soon as possible after loading of frame 4

is complete. The end of frame 5 almost exceeds the DTS time for frame 5 (DTS_5) and the buffer is in danger of overflowing. However the next few frames 6, 7 and 8 each have fewer bits than one slot so that the capacity of the buffer is alleviated.